RTL8671B/ RTL8671BH

Integrated ADSL2+ Router Controller

Datasheet

Rev. 0.4
6 May, 2008
Track ID: xxxx-nnnn-nn

Realtek Semiconductor Corp.
No. 2, Industry E. Rd. IX, Science-Based Industrial Park, Hsinchu 300, Taiwan
Tel: +886-3-5780211 Fax: +886-3-5776047
www.realtek.com.tw

USING THIS DOCUMENT

This document is intended for the software engineer’s reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
0.0	2008/01/18	First release.
0.1	2008/01/23	**n** Correcting pin 113 as ‘OVDD’ **n** Block diagram added
0.2	2008/01/30	**n** Correcting pin 12 as ‘VSS’
0.3	2008/01/31	**n** Correcting polarity of ‘U1ID’
0.4	2008/05/06	**n** ‘U1ID’ should be input only, not I/O **n** RTL8671BH added

Table of Contents

List of Tables

List of Figures

1. General Description

The Realtek **RTL8671B/ RTL8671BH** are integrated SoC featuring a RISC, an ADSL2+ Discrete Multi-tone (DMT) data-pump, a hardware-based ATM Segmentation and Reassembly (SAR), two 10/100Mbps IEEE 802.3 compliant MACs with an embedded Ethernet transceiver, and a USB PHY port. Mated with the Realtek **RTL8271B** (ADSL2+ Analog Front End), **RTL8671B/ RTL8671BH** provide a low cost integrated solution for ADSL2+ CPE modems, routers, or gateways.

RTL8671B/ RTL8671BH encompass high-performance DSP technologies, optimized mix-signal designs, and an efficient architecture to provide a seamless WAN to LAN router controller. The embedded RISC network processor supports the MIPS I instruction set along with DSP extensions and achieves a 340MHz clock rate in a six-stage pipeline to support layer 2, 3, and other upper layer applications.

The DMT engine supports the upstream data rate from 32kbp to above 3Mbps and the downstream data rate from 32kbps to above 24Mbps throughput, and complies with:

- ANSI T1.413 Issue 2
- ITU-T G.992.1 (G..dmt) Annexes A and B
- G.992.2 (G..lite) Annexes A and B
- G.992.3 ADSL2 (G.dmt.bis) Annexes A, B, I, J, L, and M
- G.992.4 ADSL2 (G.lite.bis)
- G.992.5 ADSL2+

The Ethernet interface offers high-speed transmission over CAT-5 UTP cable or CAT-3 UTP (10Mbps only) cable. Ethernet functions such as Crossover Detection & Auto-Correction and polarity correction are implemented to provide robust transmission and reception capability at high speeds.

2. Features

- Two-chip ADSL2+ CPE solution: **RTL8671B/ RTL8671BH** (ADSL2+/Network Processor SoC) + **RTL8271B** (ADSL2+ Analog Front End).
- Field proven DMT data-pump complies with ANSI T1.413 Issue 2, ITU-T G992.1, G.992.2 , G.992.3, G.992.4, G.992.5 supporting Annexes A, B, I, J, L, and M. Supports S=1/3 coding.
- High performance embedded RISC with MMU, TLB and DSP instruction extension.
- Embedded hardware-based ATM SAR: up to 8 distinct VCs—ATM AAL5 adaptation, F4/F5 OAM cell, HEC, CRC, IP/TCP/UDP checksum offloading, and error packet filtering— and QoS supported for CBR, UBR, rt-VBR, and nrt-VBR.
- Embedded 10/100 Base-TX Ethernet MAC and transceiver supporting Crossover Detection & Auto-Correction and polarity correction, IP/TCP/UDP checksum offload supported as well.
- One on-chip USB PHY port supporting the host/device mode
- Support serial SPI interface for device control
- Network device management via HTTP, SNMP, and CLI (UART).
- IP layer processing, DHCP, NAT, and typical higher layer applications supported
- 16-bit-wide, 166MHz SDRAM support up to 256Mb
- 8/16-bit-wide parallel/SPI Flash support up to 128Mb
- 3.3V signaling, 1.2V core voltage; a embedded linear regulator controller to reduce an external LDO
- Two 32-bit timers and a watchdog timer
- Embedded “Dying-Gasp” detection circuit
- EJTAG interface
- Package of 128-pin LQFP available

3. System Applications

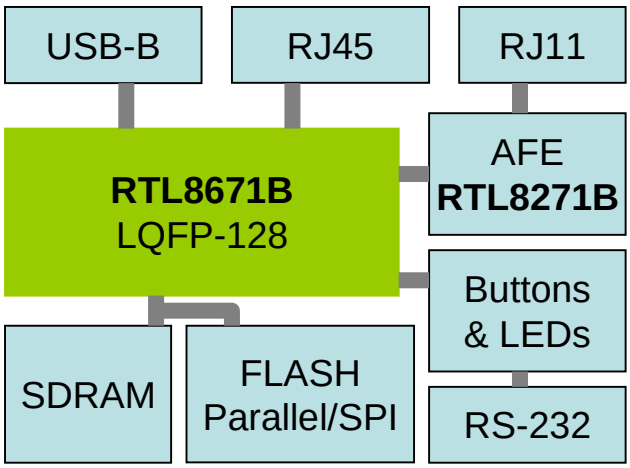


Figure 1 Application Diagram I

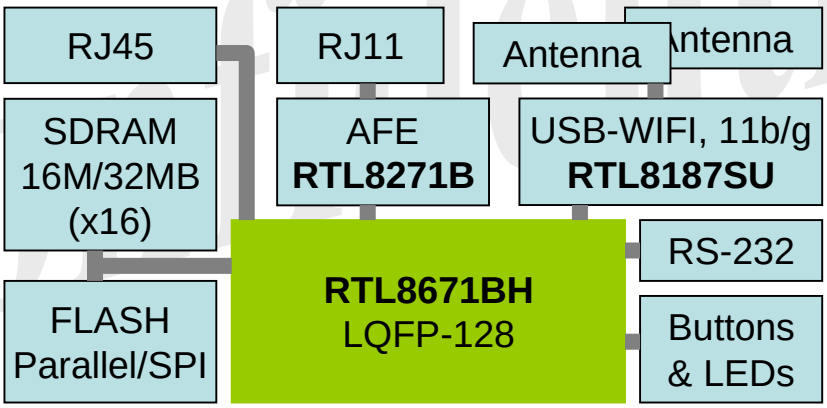


Figure 2 Application Diagram II

4. Block Diagram

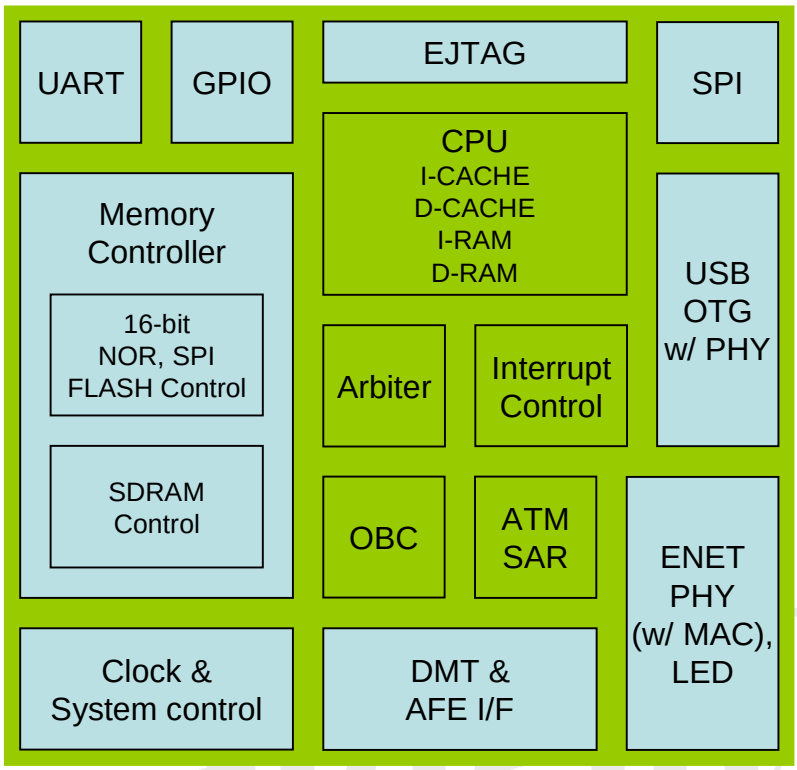


Figure 3 Block Diagram

5. Pin Assignments

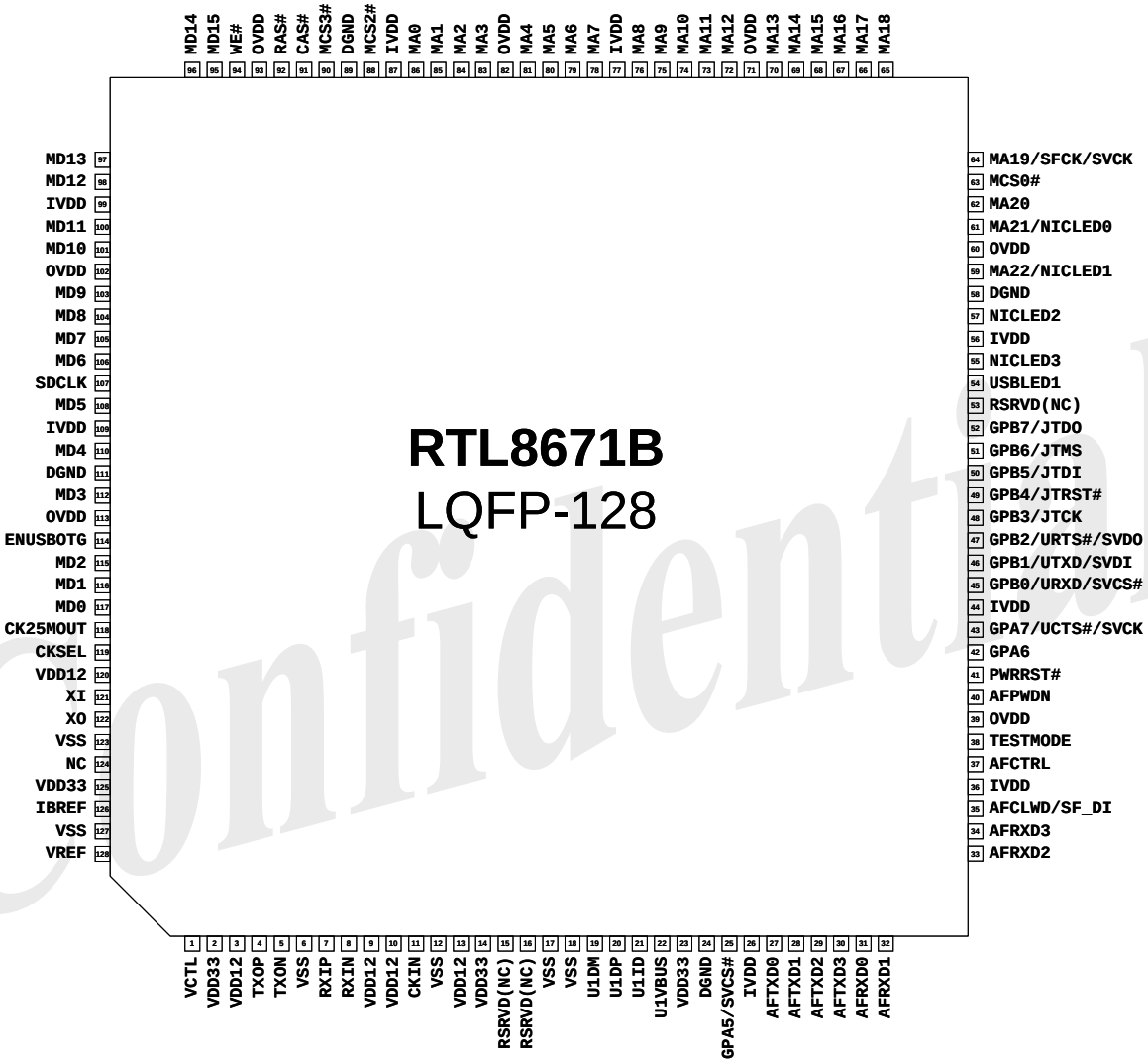


Figure 4 Pin-out Diagram

6. Pin Descriptions

Table 1 Pin Descriptions of RTL8671B/ RTL8671BH (128-pin LQFP)

Symbol	128 Pin#	Type	Description
100/10 Physical Layer			
RXIP RXIN	7 8	I	Ethernet physical layer differential RX pins
TXOP TXON	4 5	O	Ethernet physical layer differential TX pins
IBREF	126	I	Pull-down externally with 2.5k Ohm for PHY reference
Ethernet PHY LED			
NICLED[3:0]	55, 57, 59, 61	O	LED driving signals for the embedded Ethernet PHY; Pins MA[22:21] sharing with NICLED[1:0]
Clock & Reset			
XI	121	I	25MHz crystal clock input.
XO	122	O	25MHz crystal clock output.
CKSEL	119	I	Reference clock selection; tied to 1.2 to select XO (25MHz), VSS to select CKIN (35.328MHz)
PWRRST#	41	I	System reset.
SPI Control Interface			
SVCS#	45	O	SPI chip select pin (shared with GPB0 and URXD)
SVDI	46	I	SPI data in (shared with GPB1 and UTXD)
SVDO	47	O	SPI data out (shared with GPB2 and URTS#)
SVCK	48	O	SPI reference clock (shared with GPA7 and UCTS#)
USB Interface			

U1DP, U1DM	20, 19	I/O	Differential data I/O of USB PHY 1 To **RTL8671BH**: either host/device mode supported; configured by **U1ID** To **RTL8671B**: device mode supported only
U1ID (NC)	21	I	To **RTL8671BH**: Pull-low/high to select PHY 1 as host/device To **RTL8671B**: NC
U1VBUS	22	I	USB VBUS detect pin; used for PHY 1 configured in device mode
USBLED1	54	O	USB LED driver output
ENUSBOTG	114	O	Enable USB OTG block
AFE Interface			
AFPWDN	40	O	Power down control to AFE
AFRXD[3:0]	34, 33, 32, 31	I	Data input from AFE
AFTXD[3:0]	30, 29, 28, 27	O	Data output to AFE Pins AFTXD[3:2] strap into register values as OCCLK_SEL[1:0], which defines the CPU speed. For **RTL8671B/ RTL8671BH**, the AFTXD[3:2] should be strictly pulled as '10'.[1]
AFCLWD	35	I	Word clock input from AFE
CKIN	11	I	Master clock from AFE
AFCTRL	37	O	Control data output to AFE
VREF	128	I	Dying Gasp voltage detect input
Memory Bus			
MD[15:0]	95, 96, 97, 98, 100, 101, 103, 104, 105, 106, 108, 110, 112, 115, 116, 117	I/O	Data for SDRAM, parallel Flash, and ROM
MA[22:0]	59, 61, 62, 64, 65, 66, 67, 68, 69, 70, 72, 73, 74, 75, 76, 78, 79, 80, 81, 83, 84, 85, 86	O	Address for SDRAM and Flash. Pins MA[10:8] strap into register values as OCCLK_SEL[4:2], which defines the CPU speed. For **RTL8671B/ RTL8671BH**, the MA[10:8] should be strictly pulled as '001'.[1]

SDCLK	107	O	SDRAM clock
MCS2#	88	O	Bank 0 chip select SDRAM chip select.
MCS3#	90	O	Bank 1 chip select SDRAM chip select
OE#/RAS#	92	O	Raw address strobe for SDRAM interface; output enable for FLASH interface
CAS#	91	O	Column address strobe
WE#	94	O	Write enable for SDRAM/ FLASH interface
DQM[3:0]	66, 65, 68, 67	O	DQM[3:0] for SDRAM; shared with AA17, AA18, AA15, AA16
MCS0#	63	O	ROM Bank 0 chip select for FLASH memory
SFCS#	63	O	Chip select of SPI FLASH interface if enabled (AFPWDN pull-up on power-on reset)
SFDI	35	I	Serial data in of SPI FLASH interface if enabled; shared with AFCLWD
SFDO	62	O	Serial data out of SPI FLASH interface if enabled; shared with MA20
SFCK	64	O	Reference clock of SPI FLASH interface if enabled; shared with MA19
GPIO			
GPIOA[7:5]	43, 42, 25	I/O	GPIO port A
GPIOB[7:0]	52, 51, 50, 49, 48, 47, 46, 45	I/O	GPIO port B
UART			
UCTS#	43	I	Clear to send; shared with GPA7 and SV_CK
URXD	45	I	RX data; shared with GPB0 and SV_CS#
UTXD	46	O	TX data; shared with GPB1 and SV_DI

URTS#	47	O	Request to send; shared with GPB2 and SV_DO
JTAG (shared with GPIOB7-3)			
JTCK	48	I	JTAG test clock; shared with GPB3
JTMS	51	I	JTAG test mode select; shared with GPB6
JTDO	52	O	JTAG test data output; shared with GPB7
JTDI	50	I	JTAG test data in; shared with GPB5
JTRST#	49	I	JTAG test reset; shared with GPB4
POWER & GND			
VDD12	3, 9, 10, 13, 120	P	Analog 1.2V supply
VDD33	2, 14, 23, 125	P	Analog 3.3V supply
VSS	6, 12, 17, 18, 123, 127	P	Analog ground
DGND	24, 58, 89, 111	P	Digital ground
OVDD	39, 60, 71, 82, 93, 102, 113	P	3.3V digital I/O supply
IVDD	26, 36, 44, 56, 77, 87, 99, 109	P	1.2V digital kernel supply
Misc			
CK25MOUT	118	O	Clock output of 25MHz for possible peripheral use
VCTRL	1	O	Output of the embedded regulator controller to generate 1.2V VDD for the kernel supply of the chip. Connecting to an external PNP-BJT base if used (BJT collector output to IVDD); leaving no connection if not used.
DTEST	124	-	No used; leaving no connection
TESTMODE	38	I	Test only; leaving no connection Pulled-down internally for normal operation
RSRVD(NC)	15, 16, 53	-	No used; leaving no connection

Notes

1. *MA[10:9] and AFTXD[3:2] strap into the register at the power-on reset to configure the CPU speed. The value '00110' configures the CPU running at 340MHz. This is a strict setting for **RTL8671B/ RTL8671BH.** That is, AFTXD3 and MA8 should be pulled up via a 4.7k Ohm resistor, and AFTXD2 and MA[10:9] should be pulled low via a 4.7k Ohm resistor.*

7. System Overview

TBD

8. Electrical Requirements

8.1. DC Characteristics

8.1.1. Absolute Maximum Rating

Table 2 Absolute Maximum Rating

Parameters	Symbol	Min	Max	Unit
I/O supply voltage	V_{DDIO}	TBD	TBD	V
Core supply voltage	V_{DDC}	TBD	TBD	V
Storage temperature	T_{STG}		TBD	
ESD protection	VESD		TBD	V

8.1.2. Recommended Operation Conditions

Table 3 Recommended Operation Conditions

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Operating temperature	T_A	Ambient	TBD	TBD	TBD	°C
Digital supply for I/O ring	V_{DDR}		TBD	3.3	TBD	V
Core power supply voltage	V_{DDC}		TBD	1.2	TBD	V
Input high voltage	V_{IH}		TBD			V
Input low voltage	V_{IL}				TBD	V
Input current	V_{IN}		TBD		TBD	µA

8.1.3. Power Consumption

Table 4 Power Consumption

Parametes	Symbol	Condition	Estimated Power	Unit
Digital supply for I/O ring (3.3V)*	V_{DDR}	ADSL (ADSL2+ interleaved mode), and Ethernet are active	TBD	mA

Core power supply voltage (1.2V)	V_{DDC}	ADSL (ADSL2+ interleaved mode), and Ethernet active	TBD	mA
Phy power supply voltage (1.2V)	V_{DDPhy}	ADSL (ADSL2+ interleaved mode), and Ethernet are active	TBD	mA

8.1.4. Reference Crystal

Table 5 Reference Crystal

Parameters	Symbol	Min	Typ	Max	Unit
Center frequency	f_{cf}		25		MHz
Shunt capacitance	C_o				pF
Load capacitance	C_L				pF
Crystal equivalent serial resistor	C_{ESR}				Ω
Aging					ppm/yr
Frequency tolerance			+/-50		ppm

8.1.5. ADSL Interface Clock Input

Table 6 ADSL Interface Clock Input

Parameters	Symbol	Min	Typ	Max	Unit
Clock frequency	f_{clock}		35.328		MHz
Pulse duration high	$t_{w(HI)}$		14.15		ns

8.2. AC Characteristics

8.2.1. FLASH – Parallel

Table 7 Parallel FLASH Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{CS}	The timing interval between F_CS0#(or F_CS1#) and WE#	Controlled by Reg. 0xB9000004(MTCR0)			ns	

T_{WP}	The timing interval for WE# to pulled low (RAS# for read operation).	Controlled by Reg. 0xB9000004 (MTCR0)	ns	

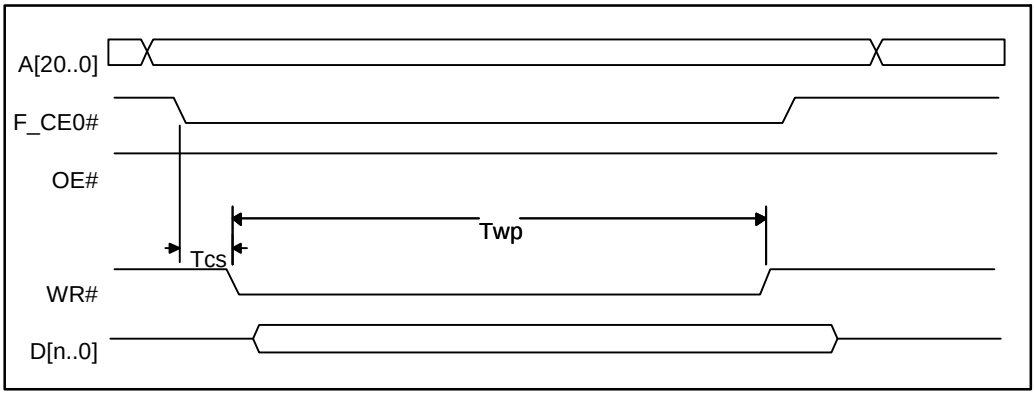


Figure 5 Flash Access Timing

8.2.2. FLASH – Serial

TBD

8.2.3. SDRAM

8.2.3.1 SDRAM Input Timing

Table 8 SDRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{SETUP}	Input setup prior to rising edge of clock. Inputs included in this timing are D[31: 0] (during a read operation)	TBD			ns	
T_{HOLD}	Input hold-time after the rising edge of clock. Inputs include in this timing are D[31: 0] (during a read operation)	TBD		TBD	ns	

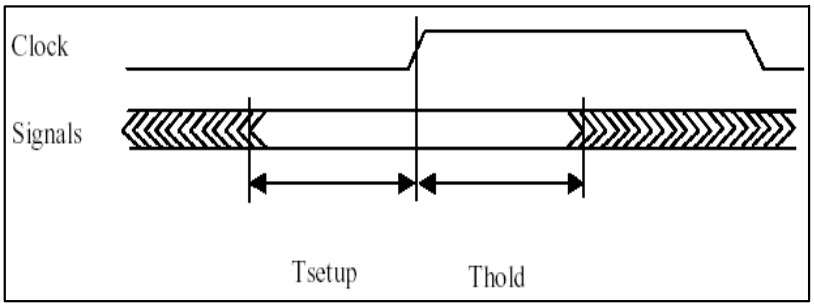


Figure 6 SDRAM Input Timing

8.2.3.2 SDRAM Output Timing

Table 9 SDRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{CLK2OUT}$	Rising edge of clock-to-signal output. Outputs include this timing are D[31: 0], CS0#, CS1#,RAS#, CAS#, LDQM, UDQM, WE# (during a write operation).	TBD		TBD	ns	
$T_{HOLDOUT}$	Signal output hold time after the rising edge of the clock. Outputs included in this timing are D[31: 0] (during a write operation).	TBD		TBD	ns	

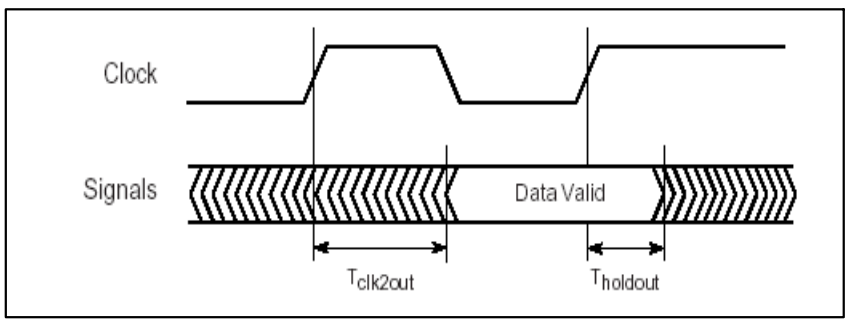


Figure 7 SDRAM Output Timing

8.2.3.3 SDRAM Access Control Timing

Table 10 SDRAM Access Control Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{REFRESH}$	Auto-refresh timing				µs	
T_{RCD}	The time interval between RAS# active and CAS# active	TBD			ns	
T_{RP}	The time interval between pre-charge and the next active	TBD			ns	
T_{RAS}	The time interval between active and pre-charge	TBD			ns	
T_{RC}	The time interval between active and the next active	TBD			ns	
T_{RFC}	The time interval between auto-refresh and active	TBD			ns	
$T_{CAS\_LATENCY}$	The data output delay after The CAS# active	TBD			ns	

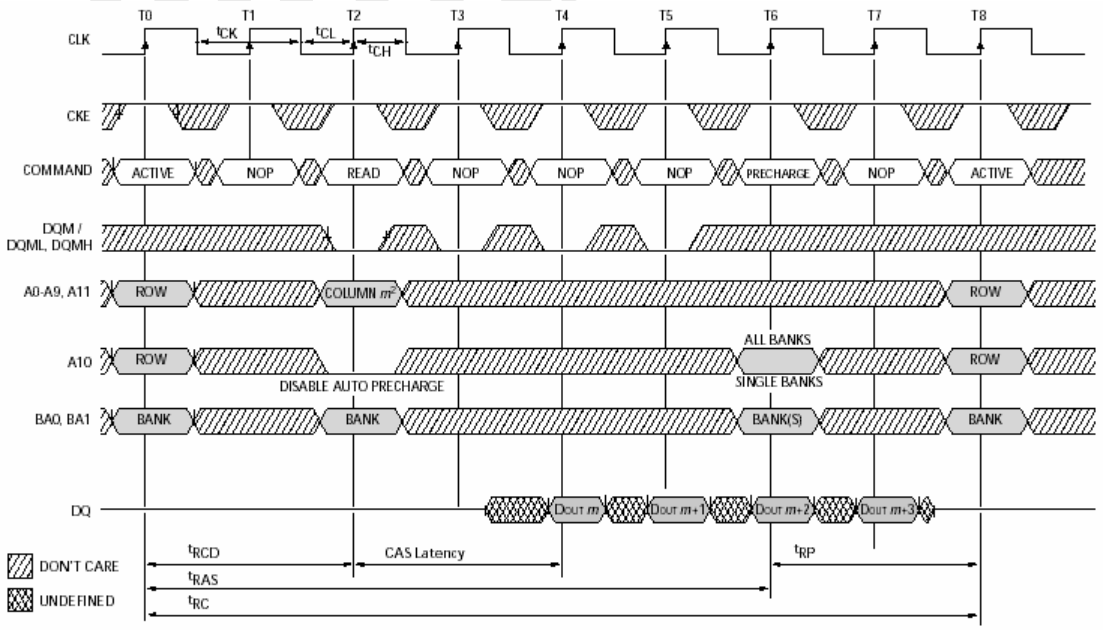


Figure 8 SDRAM Access Control Timing

8.2.4. AFE

8.2.4.1 Master clock

Table 11 AFE Master Clock

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
F	Clock frequency		35.328		MHz	
T_h	Clock duty cycle		50		%	

8.2.4.2 Transmission Interface

Table 12 AFE TX Interface

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
Tva_r	Setup time before falling edge of clock.	12		18	ns	AFE latch data at falling edge of clock

8.2.4.3 Reception Interface

Table 13 AFE RX Interface

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_s	Data setup-time prior to falling edge of clock	3			ns	
T_h	Data hold-time after falling edge of clock	3			ns	

8.2.5. JTAG

Table 14 JTAG Interface Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{BSCL}	JTAG clock low time				ns	
T_{BSCH}	JTAG clock high time				ns	
T_{BSIS}	TDI, TMS setup time to rising edge of TCK				ns	

T_{BSIH}	TDI, TMS hold time from rising edge of TCK				ns	
T_{BSOH}	TDO hold time after falling edge of TCK				ns	
T_{BSOD}	TDO output from falling edge of TCK				ns	
T_{BSR}	JTAG reset period				ns	
T_{BSRS}	TMS setup time to rising edge of JTAG reset				ns	
T_{BSRH}	TMS hold time from rising edge of JTAG reset				ns	

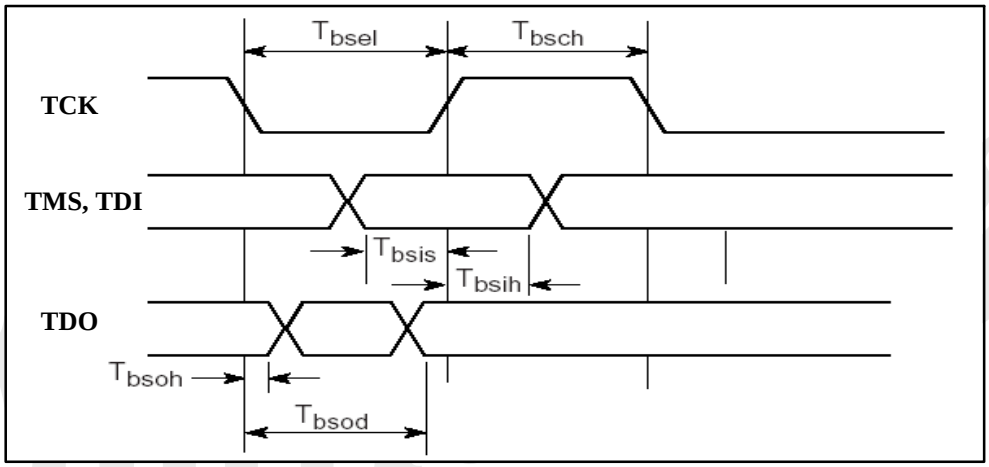


Figure 9 Boundary-Scan General Timing

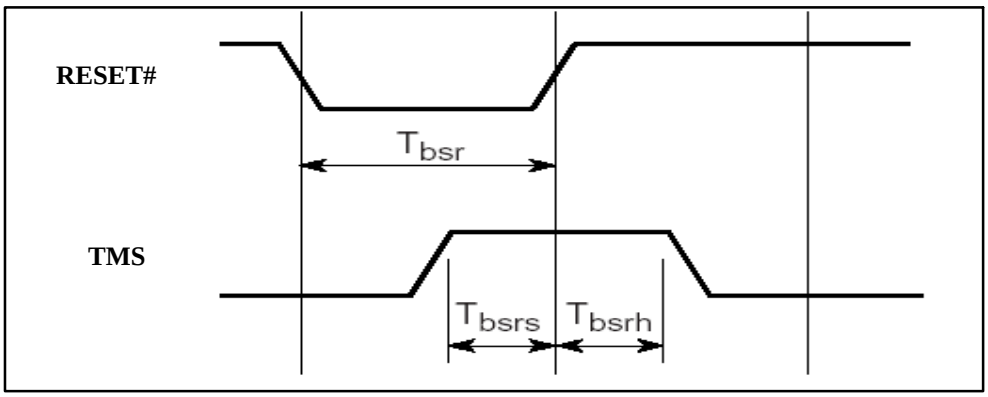


Figure 10 Boundary-Scan Reset Timing

8.2.6. Reset

Table 15 Reset Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{POWERON\_RESET}$	Minimum time required to hold the PWRRST# at logic 0 state after stable power has been applied to **RTL8671B/ RTL8671BH**		TBD		µs	
T_{PUSH_ESET}	Minimum time required to hold the PWRRST# at logic 0 state for **RTL8671B/ RTL8671BH** system reset		TBD		µs	

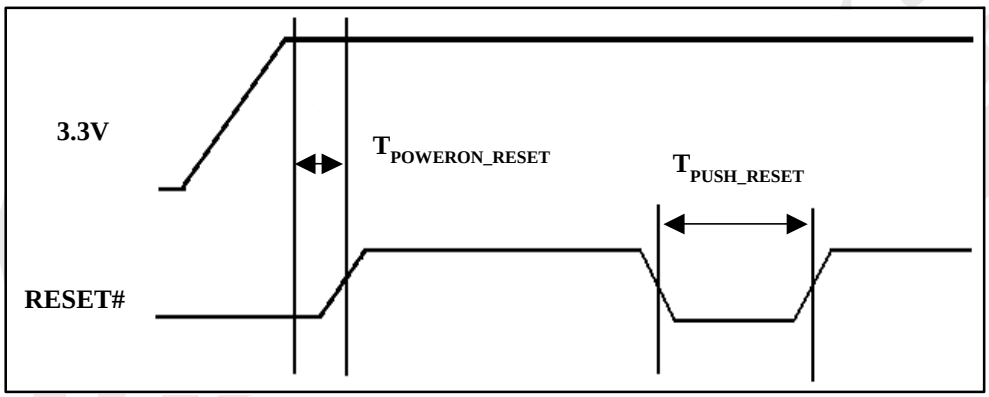


Figure 11 Reset Timing

8.2.7. V_{REF} Timing

Table 16 V_{REF} Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{delay}	Delay time from dying gasp detect to ADSL dying gasp indication bit clear		TBD		us	1
T_{RP}	Required residual power sustain time				ms	

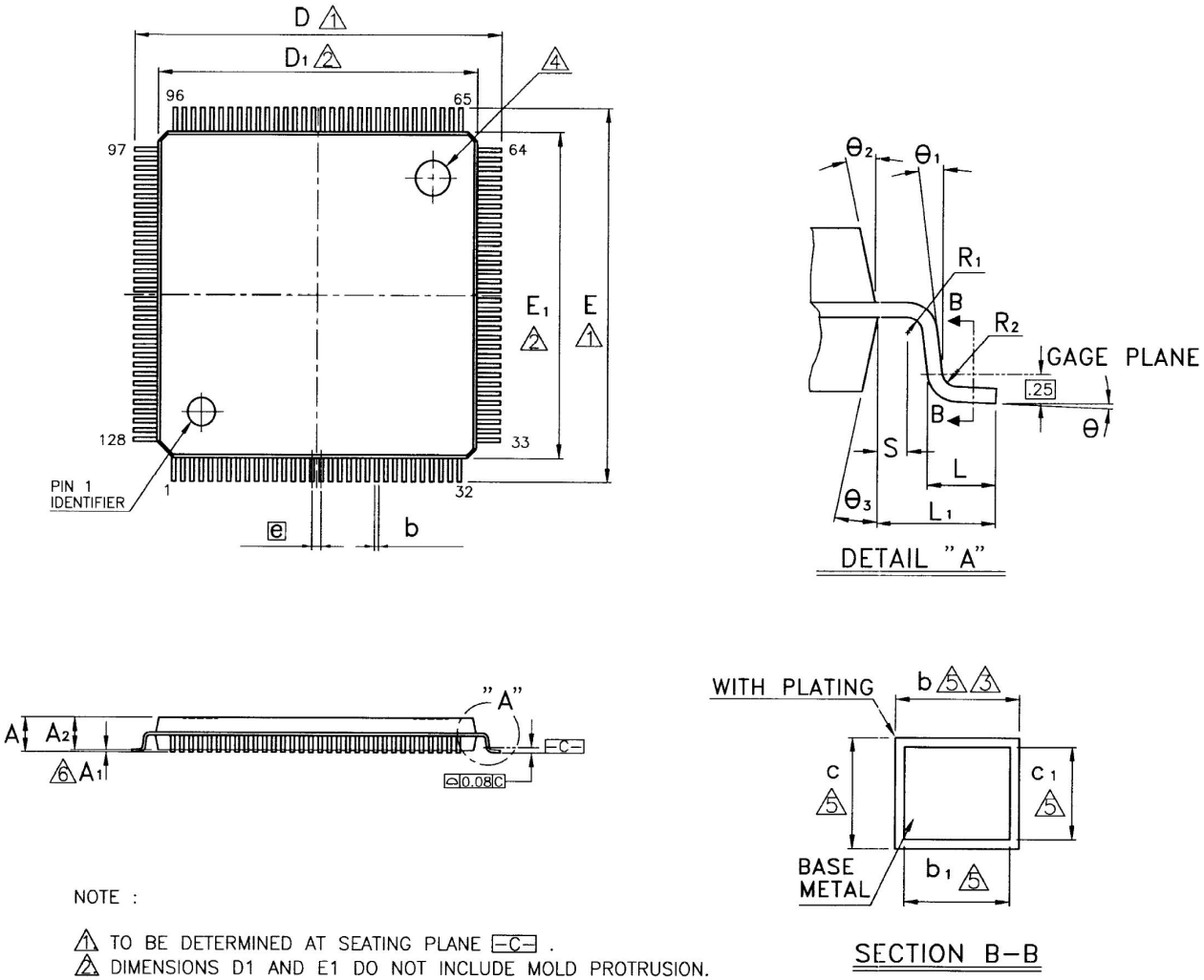
*Note1: 250*8*[(B+1)*M+R]*Tp*SEQ*D/(Lp*M)*

8.2.8. Power-on sequence

TBD

9. Mechanical Dimensions

Figure 12 Drawing of LQFP-128



NOTE :

1. TO BE DETERMINED AT SEATING PLANE -C- .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.

Table 17 Dimension of LQFP-128

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A_1	0.05	—	—	0.002	—	—
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D_1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E_1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	12°TYP			12°TYP		
$θ_3$	12°TYP			12°TYP		

10. Ordering Information

TBD

Realtek Semiconductor Corp.
Headquarters
No. 2, Innovation Road II, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
www.realtek.com.tw